WHAT IS CLAIMED IS:

1. An ~~organic electroluminescent display (OELD)~~, comprising:

a plurality of data lines for transmitting data voltages for representing image signals;

a plurality of scan lines for transmitting select signals; and

a plurality of pixel circuits respectively formed on a plurality of pixels defined by the data lines and the scan lines,

wherein each of the pixel circuit comprises:

an organic electroluminescent (EL) element for emitting light corresponding from a supplied current;

a first switch for switching data voltage supplied to a data line in response to a select signal supplied to a scan line;

a first thin film transistor (TFT) for supplying the current to the organic EL element in response to the data voltage supplied to a gate of the first TFT via the first switch;

a second TFT having a gate coupled to the gate of the first TFT and compensating for a threshold voltage deviation of the first TFT; and

a capacitor for maintaining the data voltage supplied to the gate of the first TFT during a predetermined time.

2. The OELD of claim 1, wherein the OELD further comprises a second switch for initializing the data voltage supplied to the gate of the first TFT in response to a control signal.

3. The ~~OELD~~ of claim 2, wherein the control signal is an additional

external reset signal.

4. The OELD of claim 2, wherein the control signal is a select signal of a previous scan line.

5. The OELD of claim 4, wherein the data voltage is supplied to the data line before the select signal is supplied to the pixel.

6. The OELD of claim 2, wherein a gate and a drain of the second TFT are coupled together.

7. The OELD of claim 2, wherein the first switch is a third TFT having a gate coupled to the scan line, a source coupled to the data line, and a drain coupled to a source of the second TFT, and the second switch is a fourth TFT having a gate coupled to the control signal, a source coupled to the gate of the first TFT, and a drain to which a predetermined voltage for a resetting is supplied.

8. The OELD of claim 7, wherein the predetermined voltage supplied to the drain of the fourth TFT is a ground voltage.

9. The OELD of claim 7, wherein the predetermined voltage supplied to the drain of the fourth TFT is a pre-charge voltage.

10. The OELD of claim 9, wherein the pre-charge voltage is set to be less than the minimum data voltage supplied to the gate of the first TFT so as to represent the maximum gray level.

11. The OELD of claim 7, wherein the gate and the drain of the fourth TFT

are coupled together.

12. The OELD of claim 7, wherein the first TFT, the second TFT, the third TFT and the fourth TFT have an identical conductive type.

13. The OELD of claim 7, wherein the first TFT, the second TFT and the third TFT are first conductive type transistors, and the fourth TFT is a second conductive type transistor which has a polarity opposite to that of the first conductive type transistors.

14. The OELD of claim 7, wherein the first TFT and the second TFT are first conductive type transistors, and the third TFT and the fourth TFT are second conductive type transistors which have polarity opposite to that of the first conductive type transistors.

15. The OELD of claim 1, wherein the first TFT and the second TFT have almost identical threshold voltages.

16. The OELD of claim 15, wherein the first TFT and the second TFT are parallel to the data line or the scan line, and formed on a same line.

17. A method for driving an organic electroluminescent display (OELD) including a plurality of data lines, a plurality of scan lines crossing the data lines, and a plurality of matrix type pixels having thin film transistors (TFTs) formed in regions defined by the data lines and the scan lines and supplying current to organic electroluminescent (EL) elements, comprising the steps of:

supplying a data voltage for representing image signals to the data lines;

sequentially supplying a select signal for selecting a pixel row to the scan lines;

switching the data voltage supplied to the data lines in response to the select signal, and compensating the supplied data voltage to reduce a threshold voltage deviation of the TFT; and

transmitting the compensated data voltage to a gate of the TFT, and supplying the current to the organic EL element.

18. The method of claim 17, further comprising the step of initializing the data voltage supplied to the gate of the TFT in response to a control signal.

19. The method of claim 18, wherein the control signal is an additional external reset signal.

20. The method of claim 18, wherein the control signal is a select signal of a previous scan line.

21. The method of claim 20, wherein the data voltage is supplied to the data line before the select signal is supplied to the scan line.

22. An organic electroluminescent display (OELD) pixel circuit formed on a plurality of pixels defined by a plurality of data lines and scan lines, comprising:

an organic electroluminescent (EL) element;

a first thin film transistor (TFT) having a drain coupled to the organic EL element;

a second TFT having a gate coupled to a gate of the first TFT, and the gate and a drain of the second TFT being coupled together;

a first switch having a control terminal coupled to the scan line, and having a first terminal and a second terminal respectively coupled to the data line and a source of the second TFT; and

a capacitor coupled between the gate and a source of the first TFT.

23. The pixel circuit of claim 22, wherein the pixel circuit further comprises a second switch having a control terminal to which a control signal is supplied, a first terminal coupled to the drain of the second TFT, and a second terminal to which a predetermined voltage is supplied.

24. The pixel circuit of claim 23, wherein an additional external reset signal is supplied to the control terminal of the second switch.

25. The pixel circuit of claim 23, wherein a previous scan line is coupled to the control terminal of the second switch.

26. The pixel circuit of claim 23, wherein the first switch is a third TFT having a gate coupled to the scan line, a source coupled to the data line, and a drain coupled to a source of the second TFT, and the second switch is a fourth TFT having a gate for responding to the control signal, a source coupled to the gate of the first TFT, and a drain to which a predetermined voltage for a reset process is supplied.

27. The pixel circuit of claim 26, wherein the gate and the drain of the fourth TFT are coupled together.

28. The pixel circuit of claim 26, wherein the first to fourth TFTs have an identical conductive type.

29. The pixel circuit of claim 26, wherein the first TFT, the second TFT and the third TFT are first conductive type transistors, and the fourth TFT is a second conductive type transistor which has a polarity opposite to that of the first conductive type transistors.

30. The pixel circuit of claim 26, wherein the first TFT and the second TFT are first conductive type transistors, and the third TFT and the fourth TFT are second conductive type transistors which have polarity opposite to that of the first conductive type transistors.

31. The pixel circuit of claim 22, wherein the first TFT and the second TFT have almost identical threshold voltages.

32. The OELD of claim 3, wherein the first TFT and the second TFT are parallel to the data line or the scan line, and formed on the same line.

33. The OELD of claim 2, wherein the first switch is a third TFT having a gate coupled to the scan line, a drain coupled to the data line, and a source coupled to a drain of the second TFT, and the second switch is a fourth TFT having a gate coupled to the control signal, a drain coupled to the gate of the first TFT, and a source to which a predetermined voltage for a resetting is supplied.

34. The pixel circuit of claim 23, wherein the first switch is a third TFT having a gate coupled to the scan line, a drain coupled to the data line, and a source coupled to a drain of the second TFT, and the second switch is a fourth TFT having a gate for responding to the control signal, a drain coupled to the gate of the first TFT,

and a source to which a predetermined voltage for a reset process is supplied.